μPD75268
4-Bit Microcomputer With FIP® (VF) Controller/Driver

Description

The μPD75268 is a low-cost, high-performance, single-chip CMOS microcomputer containing CPU, ROM, RAM, I/O ports, several timer/counters, a FIP controller, vectored interrupts, main and subsystem clocks, and serial interface. The devices are ideally suited for controlling VCRs, microwave ovens, electronic stoves, washing machines, electronic cash registers, audio equipment, and meters.

(For the programmable equivalents, use μPD75CG216 or μPD75P216A.)

Features

- 103 instructions
  - Bit manipulation
  - 4-bit add and subtract
  - 4-bit and 8-bit transfer
  - GETI instruction, to convert one 2-byte or two 1-byte instructions into a single 1-byte instruction
  - 1-byte relative branch
- Fast execution time (@ 4.19 MHz)
  - High-speed cycle: 0.95 μs
  - Lower-voltage cycles: 1.91 and 15.3 μs
- 8064 bytes of program ROM
- 512 x 4 bits of program RAM
- Eight 4-bit registers
- 32 port lines
  - 20 general-purpose I/O, 8 outputs directly drive LEDs (I_{sink} = 15 mA rms)
  - 8 input-only lines
- Three timers
  - 8-bit basic interval timer
  - 8-bit timer/event counter
  - 14-bit watch timer with buzzer output
- Programmable FIP controller with memory area
  - Up to 16 segments
  - Up to 16 digits

FIP is a registered trademark of NEC Corporation

- 8-bit serial interface
  - Data transfer can be full duplex or receive only, and can be MSB or LSB first
- Vectored interrupts
  - Three external interrupts
  - Four internal interrupts
- Two interrupt requests
- Standby modes
  - HALT mode: stops CPU only
  - STOP mode: stops main system clock
- Operates with oscillator or ceramic resonator
- CMOS technology, with V_{DD} from 2.7 to 6.0 V

Ordering Information

Part Number	Package Type	ROM
μPD75268CW-xxx	64-pin plastic SDIP	Mask ROM
μPD75268GF-xxx-3BE	64-pin plastic QFP	Mask ROM

Note:
xxx indicates ROM code.

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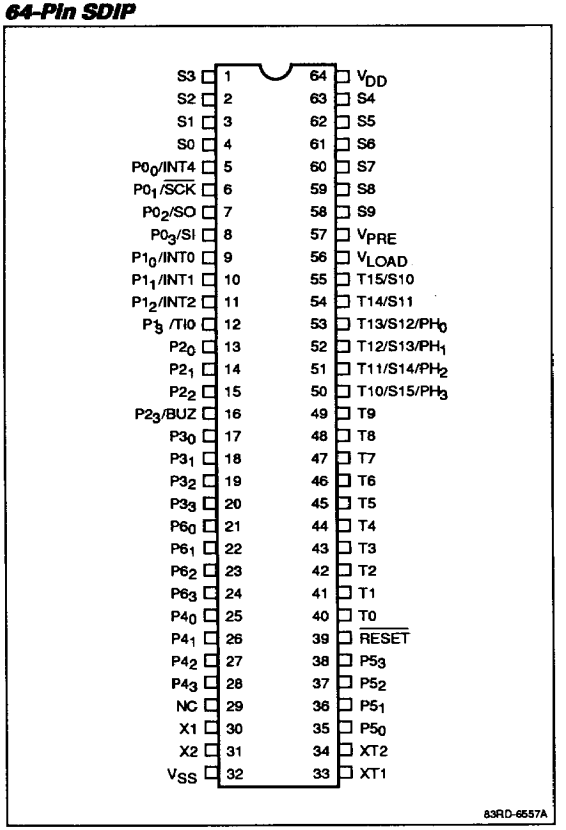
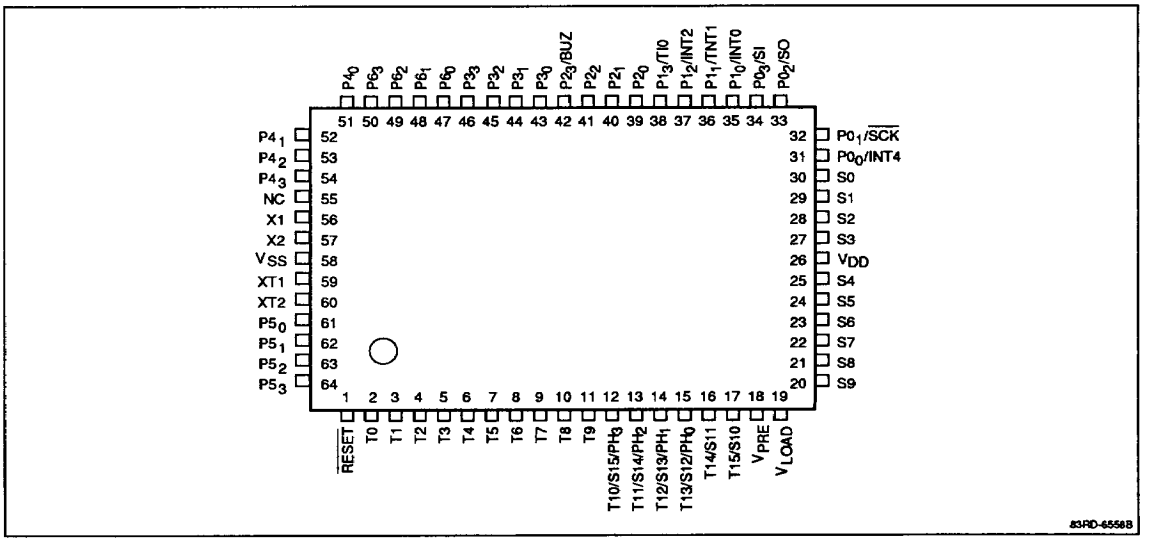
Pin Configurations

64-Pin SDIP



Pin Configurations

64-Pin QFP



Pin Identification

Symbol	Function
$P0_0$/INT4	Port 0 input; interrupt 4
$P0_1$/$\overline{SCK}$	Port 0 input; serial clock
$P0_2$/SO	Port 0 input; serial out
$P0_3$/SI	Port 0 input; serial in
$P1_0$/INT0	Port 1 input; interrupt 0
$P1_1$/INT1	Port 1 input; interrupt 1
$P1_2$/INT2	Port 1 input; interrupt 2
$P1_3$/TI0	Port 1 input; timer 0 input
$P2_0$-$P2_2$	Port 2 I/O
$P2_3$/BUZ	Port 2 I/O; buzzer output
$P3_0$-$P3_3$	Port 3 I/O
$P4_0$-$P4_3$	Port 4 I/O
$P5_0$-$P5_3$	Port 5 I/O
$P6_0$-$P6_3$	Port 6 I/O
PH_0/T13/S12	Port H output; digit select line; segment select line
PH_1/T12/S13	Port H output; digit select line; segment select line
PH_2/T11/S14	Port H output; digit select line; segment select line
PH_3/T10/S15	Port H output; digit select line; segment select line
S0-S9	FIP segment outputs
T0-T9	FIP digit select outputs

Symbol	Function
T14/S11 T15/S10	Digit selects T14 and T15; segment selects S10 and S11.
X1, X2	Main clock inputs
XT1, XT2	Subsystem clock inputs
$\overline{RESET}$	Reset input
V_{PRE}	FIP predriver negative supply voltage
V_{LOAD}	FIP high-voltage negative supply voltage
V_{DD}	Positive power supply
V_{SS}	Ground

PIN FUNCTIONS

$P0_0$/INT4, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI

These pins can be used as 4-bit input port 0. Or, $P0_0$ can also be used for vectored interrupt 4, which interrupts on either the leading edge or the trailing edge of the signal. $P0_1$-$P0_3$ may also be used for the serial interface in the 2/3 wire mode. SI is the serial input, SO is the serial output, and $\overline{SCK}$ is the serial clock. Reset causes these pins to default to the port 0 input mode.

$P1_0$/INT0, $P1_1$/INT1, $P1_2$/INT2, $P1_3$/TI0

These pins can be used as 4-bit input port 1. Or, $P1_0$ and $P1_1$ can also be used for edge-triggered interrupts INT0 and INT1. $P1_2$ can be used for INT2, which is also an edge-triggered input, but one which generates an interrupt request and does not cause an interrupt. $P1_3$ can be used as an input clock to the timer/event counter to count external events. Reset causes these pins to default to the port 1 input mode.

$P2_0$, $P2_1$, $P2_2$, $P2_3$/BUZ

These pins can be used as 4-bit I/O port 2. When used as an output, the data is latched. When used as an input port the port outputs are three-state. $P2_3$ can also be used to output square waves for a buzzer. Reset causes these pins to default to the port 2 input mode.

$P3_0$-$P3_3$, $P4_0$-$P4_3$, $P5_0$-$P5_3$

Ports 3, 4, and port 5 are 4-bit I/O ports with latched outputs. Ports 4 and 5 will directly drive LEDs. Each bit of port 3 can be independently programmed to be either an input or an output, while ports 4 and 5 can be programmed to be either an input port or an output port. A reset signal causes these ports to default to the input mode.

$P6_0$-$P6_3$

Port 6 is a 4-bit I/O port. Outputs are latched, and each bit can be independently programmed to be either an input or an output. Port 6 can have pulldown resistors added as a mask option. A reset signal causes this port to default to the input mode.

PH_0/T13/S12, PH_1/T12/S13, PH_2/T11/S14, PH_3/T10/S15

Port H is a 4-bit output-only port, with P-channel open-drain outputs capable of directly driving LEDs. Output pulldown resistors can be selected as a mask-option. Alternatively, these pins can be used as high-voltage digit/segment outputs (T13/S15 - T10/S12). A reset signal causes this port to default to the high-impedance state; if mask-option resistors are present the output goes low.

S0-S9

These are high-voltage outputs used as FIP controller segment signals. pulldown resistors can be selected as a mask-option. A reset signal sets these pins to the high-impedance state; if mask-option resistors are present the outputs go low.

T0-T9

These are high-voltage outputs used as FIP controller digit select timing signals. pulldown resistors can be selected as a mask-option. A reset signal sets these pins to the high-impedance state; if mask-option resistors are present the outputs go low.

T14/S11, T15/S10

These two pins provide additional digit or segment selectors. When not used for the display they can be used as static outputs. Internal pulldown resistors are available as a mask option.

X1, X2

These pins are the main system clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

XT1, XT2

These pins are the subsystem clock inputs. The clock can be either a ceramic resonator or a crystal; an external logic signal may also be used.

$\overline{\text{RESET}}$

This is the reset input, and it is active low.

V_{PRE}

This is the power supply for the predrivers of the FIP controller.

V_{LOAD}

This pin is used to supply power to the output drivers for the segment and digit select pins of the FIP controller.

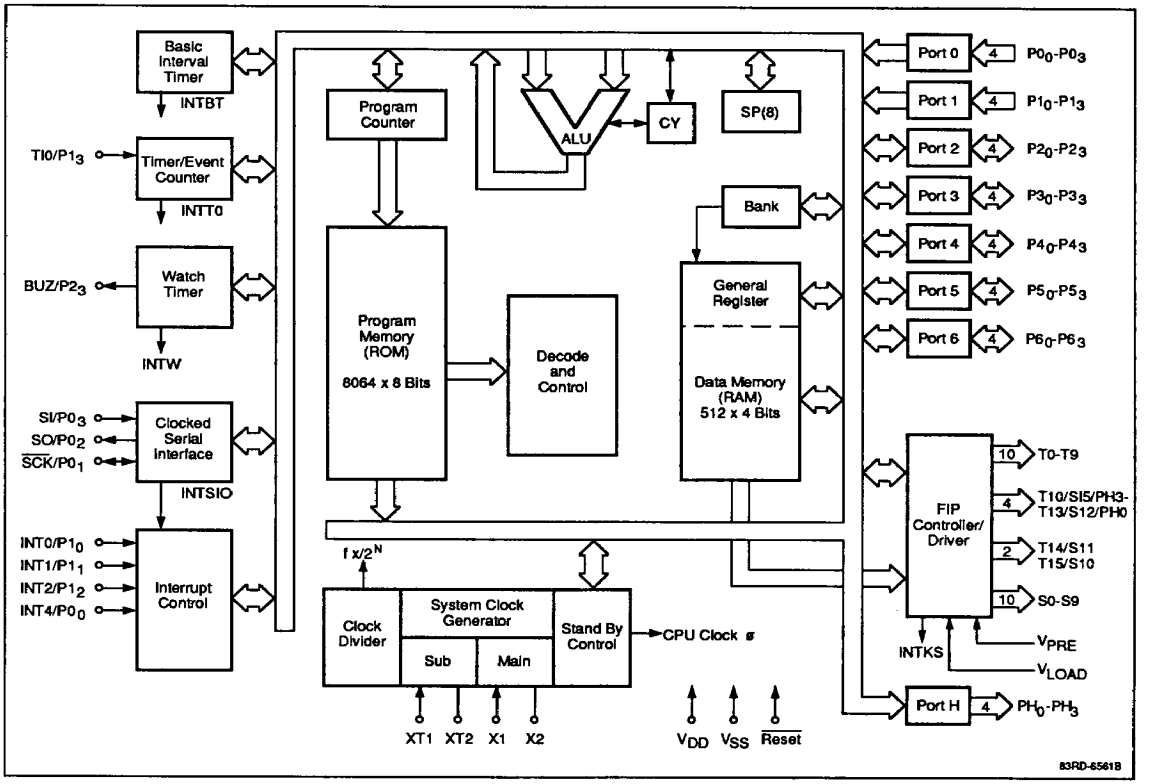
V_{DD}

The system positive power supply pin.

V_{SS}

System ground.

Block Diagram



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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.3 to +7.0 V
Supply voltage, V_{LOAD}	V_{DD} −40 to V_{DD} +0.3 V
Supply voltage, V_{PRE}	V_{DD} −12 to V_{DD} +0.3 V
Input voltage, V_{IN}	−0.3 to V_{DD} + 0.3 V
Output voltage, V_O (other than display)	−0.3 to V_{DD} + 0.3 V
Output voltage, V_{OD} (display pins)	V_{DD} −40 to V_{DD} +0.3 V
High-level output current, I_{OH} (single pin; other than display)	−15 mA
High-level output current, I_{OH} (single pin; S0-S9)	−15 mA
High-level output current, I_{OH} (single pin; T0-T15)	−30 mA
High-level output current, I_{OH} (total of all pins other than display)	−20 mA
High-level output current, I_{OH} (total of all display outputs)	−120 mA
Low-level output current, I_{OL} (single pin)	17 mA
Low-level output current, I_{OL} (total of all pins)	60 mA
Power dissipation, P_D (plastic QFP)	450 mW (Note 1)
Power dissipation, P_D (plastic SDIP)	600 mW (Note 1)
Storage temperature, t_{STG}	−65 to + 150°C
Operating temperature, t_{OPT}	−40 to +85°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) Care must be taken when designing the microcomputer that the total power dissipation does not exceed the maximum allowable. Power is dissipated in three areas:
   a. At the CPU. P_D is calculated by the product of V_{DD} (max) and I_{DD1}(max).
   b. By the output pins. Total power dissipation is the sum of the values for each pin when maximum current is applied.
   c. By the pulldown resistors.

Main System Clock Oscillator Characteristics

T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Ceramic resonator (Figure 1A)	Oscillation frequency (Note 1)	f_{XX}	2.0		5.0	MHz	
	Oscillation stabilization time (Note 2)				4 (Note 3)	ms	
Crystal resonator (Figure 1A)	Oscillation frequency (Note 1)	f_{XX}	2.0	4.19	5.0	MHz	
	Oscillation stabilization time (Note 2)				10 (Note 3)	ms	V_{DD} = 4.5 to 6.0 V
					30 (Note 3)	ms	
External clock (Figure 1B)	X1 input frequency	f_X	2.0		5.0	MHz	
	X1 input high- and low-level width	t_{XH}, t_{XL}	100		250	ns	

Notes:

(1) The oscillation frequency and X1 input frequency are included only to show the frequency range of the oscillators. Refer to the AC Characteristics table for actual instruction execution times.

(2) The oscillation stabilization time is the time required for the oscillator to stabilize after V_{DD} is applied or the STOP mode is released.

(3) Values shown are typical values for resonators. Actual values should be obtained from the manufacturer's specification sheets.

Subsystem Clock Oscillator Characteristics

T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V

Oscillator	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Crystal resonator (Figure 2A)	Oscillation frequency (Note 1)	f_{XT}	32	32.768	35	kHz	
	Oscillation stabilization time (Note 2)			1.0	2 (Note 3)	s	V_{DD} = 4.5 to 6.0 V
					10 (Note 3)	s	
External clock (Figure 2B)	XT1 input frequency	f_{XT}	32		100	kHz	
	XT1 input high- and low-level width	t_{XTH}, t_{XTL}	10		32	μs	

Notes:

(1) The oscillation frequency and X1 input frequency are included only to show the frequency range of the oscillators. Refer to the AC Characteristics table for actual instruction execution times.

(2) The oscillation stabilization time is the time required for the oscillator to stabilize after V_{DD} is applied or the STOP mode is released.

(3) Values shown are typical values for resonators. Actual values should be obtained from the manufacturer's specification sheets.

Figure 1. Main System Clock Configurations

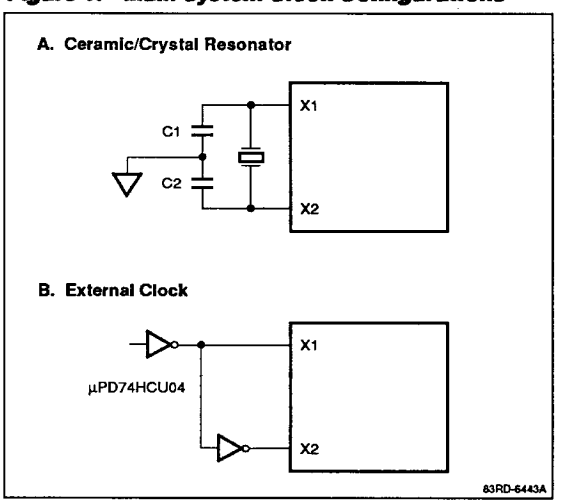
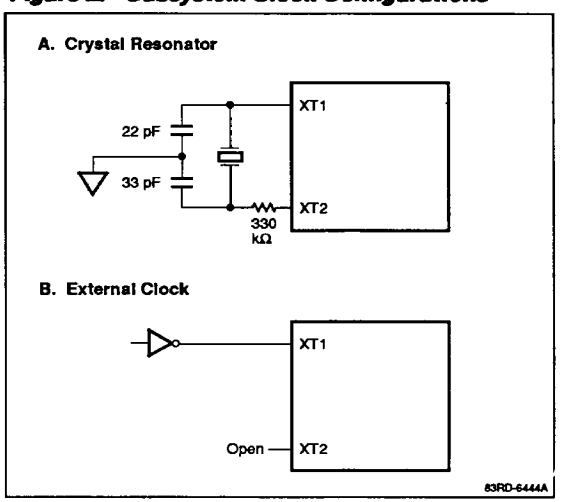


Figure 2. Subsystem Clock Configurations



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Capacitance

V_{DD} = 0 V; T_A = 25°C

Parameter	Symbol	Min	Max	Unit	Conditions
Input capacitance	C_{IN}		15	pF	f = 1 MHz All unmeasured pins returned to ground
Output capacitance; Other than display output pins	C_{OUT1}		15	pF	
Output capacitance; Display output pins	C_{OUT2}		35	pF	
I/O capacitance	C_{IO}		15	pF	

Operating Supply Voltage

T_A = −40 to +85°C

Parameter	Min	Max	Unit
CPU (Note 1)	(Note 2)	6.0	V
Display controller	4.5	6.0	V
Other hardware (Note 1)	2.7	6.0	V

Notes:

(1) The CPU does not include the system clock oscillator and the display controller.

(2) Varies according to the cycle time. See AC Characteristics.

DC Characteristics

T_A = −40 to +85°C; V_{DD} = 2.7 to 6.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
High-level input voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	V	All except ports 0 and 1; RESET; X1, X2, XT1
	V_{IH2}	0.75 V_{DD}		V_{DD}	V	Ports 0 and 1; RESET
	V_{IH3}	V_{DD}−0.4		V_{DD}	V	X1, X2, XT1
	V_{IH4}	0.65 V_{DD}		V_{DD}	V	Port 6; V_{DD} = 4.5 to 6.0 V
		0.7 V_{DD}		V_{DD}	V	Port 6; V_{DD} = 2.7 to 6.0 V
Low-level input voltage	V_{IL1}	0		0.3 V_{DD}	V	All except ports 0, 1, and 6; RESET; X1, X2, XT1
	V_{IL2}	0		0.2 V_{DD}	V	Ports 0, 1 and 6; RESET
	V_{IL3}	0		0.4	V	X1, X2, XT1
High-level output voltage	V_{OH}	V_{DD}−1.0			V	All outputs; V_{DD} = 4.6 to 6.0 V; I_{OH} = −1 mA
		V_{DD}−0.5			V	All outputs; V_{DD} = 2.7 to 6.0 V; I_{OH} = −100 μA
Low-level output voltage	V_{OL}		0.4	2.0	V	Ports 4 and 5; V_{DD} = 4.6 to 6.0 V; I_{OL} = 15 mA
				0.4	V	All output pins; V_{DD} = 4.6 to 6.0 V; I_{OL} = 1.6 mA
				0.5	V	All output pins; V_{DD} = 2.7 to 6.0 V; I_{OL} = 400 μA
High-level input leakage current	I_{LIH1}			3	μA	All except X1, X2, and XT1; V_{IN} = V_{DD}
	I_{LIH2}			20	μA	X1, X2, and XT1; V_{IN} = V_{DD}
Low-level input leakage current	I_{LIL1}			−3	μA	All except X1, X2, and XT1; V_{IN} = 0 V
	I_{LIL2}			−20	μA	X1, X2, and XT1; V_{IN} = 0 V
High-level output leakage current	I_{LOH}			3	μA	All output pins; V_{OUT} = V_{DD}
Low-level output leakage current	I_{LOL1}			−3	μA	All except display output pins; V_{OUT} = 0 V
	I_{LOL2}			−10	μA	Display output pins; V_{OUT} = V_{LOAD} = V_{DD}−35 V
Display output current	I_{OD}	−3	−5.5		mA	S0 - S9; (Note 1) and Recommended External Circuit (figure 3)
		−1.5	−3.5		mA	S0 -S9; (Note 2)
		−15	−22		mA	T0 - T15; (Note 1) and Recommended External Circuit (figure 3)
		−7	−15		mA	T0 - T15; (Note 2)

DC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Internal pulldown resistor (mask option)	R_{P6}	20	80	200	kΩ	Port 6; V_{DD} = 4.5 to 6.0 V; V_{IN} = V_{DD}
		20		1000	kΩ	Port 6; V_{DD} = 2.7 to 6.0 V; V_{IN} = V_{DD}
	R_L	25	70	135	kΩ	Display output pins; V_{DD}–V_{LOAD} = 35 V
Supply current (Note 6)	I_{DD1}		3.0	9.0	mA	V_{DD} = 5 V ± 10% (Notes 3, 4)
			0.55	1.5	mA	V_{DD} = 3 V ± 10% (Notes 3, 5)
	I_{DD2}		600	1800	μA	HALT mode; V_{DD} = 5 V ± 10% (Note 3)
			200	600	μA	HALT mode; V_{DD} = 3 V ± 10% (Note 3)
	I_{DD3}		40	120	μA	V_{DD} = 3 V ± 10% (Notes 7, 8)
	I_{DD4}		5	15	μA	HALT mode; V_{DD} = 3 V ± 10% (Notes 7, 8)
	I_{DD5}		0.5	20	μA	STOP mode; XT1 = 0V; V_{DD} = 5 V ± 10 %
			0.1	10	μA	STOP mode; XT1 = 0V; V_{DD} = 3 V ± 10 %

Notes:

(1) V_{DD} = 4.5 to 6.0 V; V_{OD} = V_{DD} –2 V; V_{PRE} = V_{DD} –9 ±1 V

(2) V_{DD} = 4.5 to 6.0 V; V_{OD} = V_{DD} –2 V; V_{PRE} = 0 V

(3) 4.19 MHz crystal oscillator; C1 = C2 = 15 pF.

(4) Value during high-speed operation; processor control clock (PCC) is set to 0011.

(5) Value during low-speed operation; processor control clock (PCC) is set to 0000.

(6) Does not include internal pulldown resistor current.

(7) 32 MHz crystal oscillator

(8) Value when the system clock control register (SCC) is set to 1001, main system clock is stopped, and the subsystem clock operates the chip.

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AC Characteristics

T_A = -40 to +85°C; V_{DD} = 2.7 to 6.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Cycle time minimum instruction execution time — (Note 1)	t_{CY}	0.95		32	μs	CPU using main system clock; V_{DD} = 4.5 to 6.0 V
		3.8		32	μs	CPU using main system clock; V_{DD} = 2.7 to 6.0 V
		114	122	125	μs	CPU using subsystem clock; V_{DD} = 2.7 to 6.0 V
TIO input frequency	f_{TI}	0		0.6	MHz	V_{DD} = 4.5 to 6.0 V
		0		165	kHz	V_{DD} = 2.7 to 6.0 V
TIO input high- and low-level width	t_{IH}, t_{IL}	0.83			μs	V_{DD} = 4.5 to 6.0 V
		3			μs	V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ cycle time	t_{KCY}	0.8			μs	Input; V_{DD} = 4.5 to 6.0 V
		0.95			μs	Output; V_{DD} = 4.5 to 6.0 V
		3.2			μs	Input; V_{DD} = 2.7 to 6.0 V
		3.8			μs	Output; V_{DD} = 2.7 to 6.0 V
$\overline{SCK}$ high- and low-level width	t_{KH}, t_{KL}	0.4			μs	Input; V_{DD} = 4.5 to 6.0 V
		$0.5t_{KCY}$–50			ns	Output; V_{DD} = 4.5 to 6.0 V
		1.6			μs	Input; V_{DD} = 2.7 to 6.0 V
		$0.5t_{KCY}$–150			ns	Output; V_{DD} = 2.7 to 6.0 V

AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
SI to $\overline{SCK}$ ↑ setup time	t_{SIK}	100			ns	
SI to $\overline{SCK}$ ↑ hold time	t_{KSI}	400			ns	
$\overline{SCK}$ ↓ to SO output delay time	t_{KSO}			300	ns	V_{DD} = 4.5 to 6.0 V
				1000	ns	V_{DD} = 2.7 to 6.0 V
Interrupt inputs high- and high-level width	t_{INTH}, t_{INTL}	(Note 2)			μs	INT0
		$2t_{CY}$			μs	INT1
		10			μs	INT2, INT4
$\overline{RESET}$ low-level width	t_{RSL}	10			μs	

Notes:

(1) Cycle time is determined by the frequency of the oscillator connected to the microcomputer, system clock control register (SCC), and the processor clock control (PCC). See the graph depicting the Supply Voltage to the cycle time (figure 4) when the microcomputer is operating on the main system clock.

(2) $2t_{CY}$ or $128/f_{XX}$, depending on the setting of the interrupt mode register (IM0).

Data Memory STOP Mode Low Voltage Data Retention Characteristics

T_A = −40 to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{DDDR}	2.0		6.0	V	
Data retention current	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2.0 V (Note 1)
Release signal SET time	t_{SREL}	0			μs	
Oscillation stabilization time (Note 2)	t_{WAIT}		(2)		ms	Release by $\overline{RESET}$ input
			(2)		ms	Release by interrupt request

Notes:

(1) Excludes current in the internal pulldown resistors.

(2) Oscillation stabilization WAIT time is the time during which the CPU is stopped and the crystal is stabilizing; consult the vendor's resonator or crystal specifications sheet for this value. This time is required to prevent unstable operation while the oscillation is started. The interval timer can be used to delay the CPU from executing instructions using the basic interval timer mode register (BTM) according to the following table:

BTM3	BTM2	BTM1	BTM0	WAIT time
–	0	0	0	$2^{20}/f_{XX}$ (Approx 250 ms)
–	0	1	1	$2^{17}/f_{XX}$ (Approx 31.3 ms)
–	1	0	1	$2^{15}/f_{XX}$ (Approx 7.82 ms)
–	1	1	1	$2^{13}/f_{XX}$ (Approx 1.95 ms)

Figure 3. Recommended External Circuit

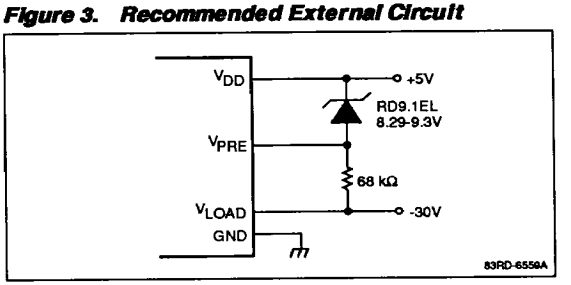
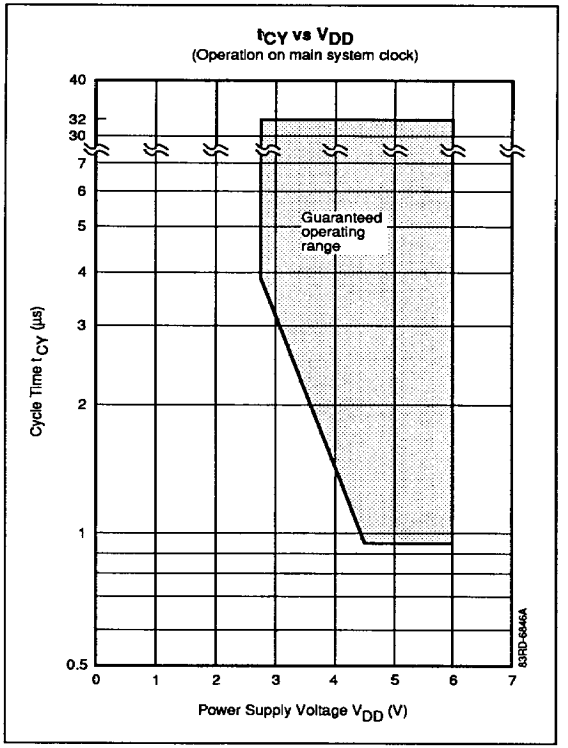
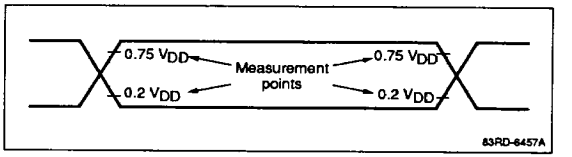


Figure 4. Guaranteed Operating Range

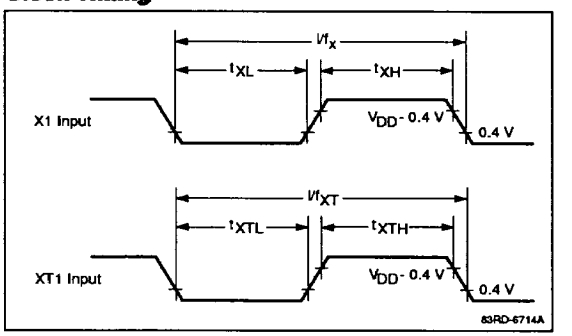


TIMING WAVEFORMS

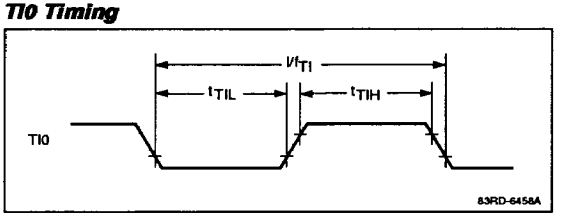
AC Timing Measurement Points (Excluding X1 and XT1 input pins)



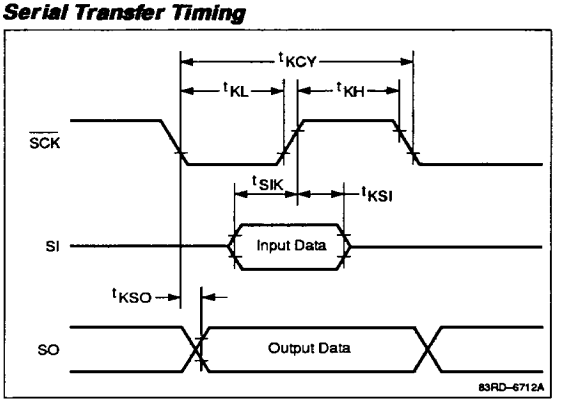
Clock Timing



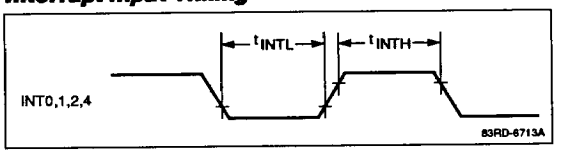
TI0 Timing



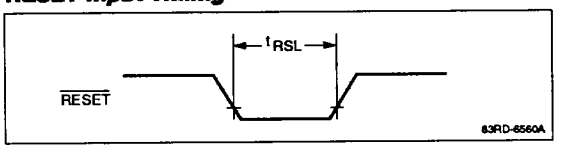
Serial Transfer Timing



Interrupt Input Timing

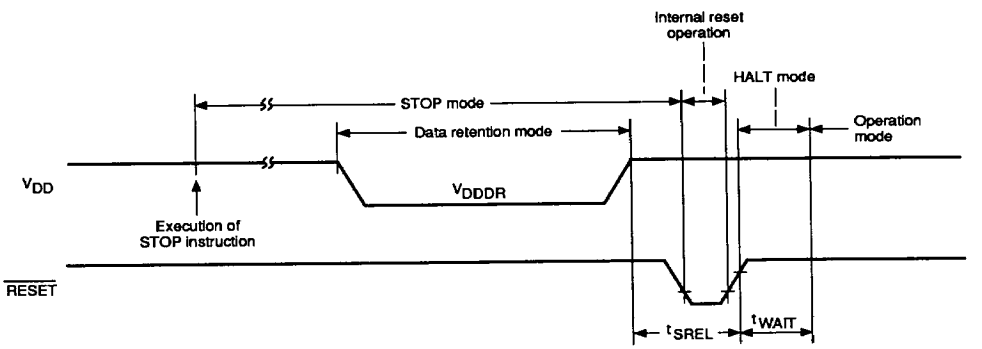


RESET Input Timing

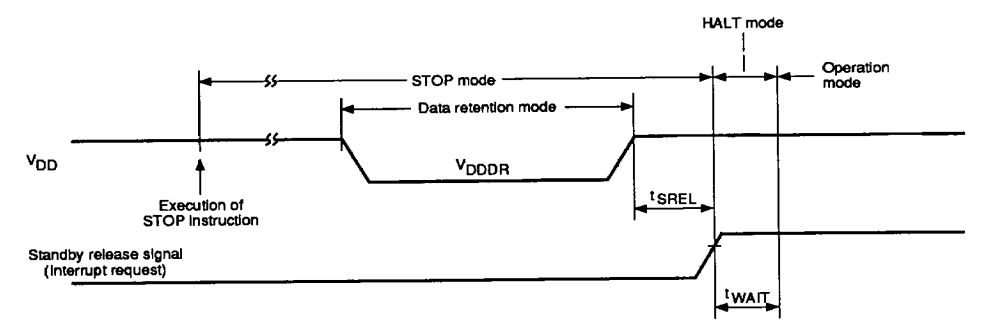


Data Retention Timing

A. STOP mode is released by RESET input



B. STOP mode is released by interrupt signal



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