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1  -----
2  -- Company:
3  -- Engineer:
4  --
5  -- Create Date:    09:39:44 06/04/2010
6  -- Design Name:
7  -- Module Name:    LCD_CTRL - Behavioral
8  -- Project Name:
9  -- Target Devices:
10 -- Tool versions:
11 -- Description:
12 --
13 -- Dependencies:
14 --
15 -- Revision:
16 -- Revision 0.01 - File Created
17 -- Additional Comments:
18 --
19  -----
20 library IEEE;
21 use IEEE.STD_LOGIC_1164.ALL;
22 --use IEEE.STD_LOGIC_ARITH.ALL;
23 --use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25 ---- Uncomment the following library declaration if instantiating
26 ---- any Xilinx primitives in this code.
27 --library UNISIM;
28 --use UNISIM.VComponents.all;
29
30 entity LCD_CTRL is
31     Port (    CLOCK          : in  STD_LOGIC;
32             ENABLE          : in  STD_LOGIC;
33             D_C              : in  STD_LOGIC;
34             LCD_DATA         : in  STD_LOGIC_VECTOR (7 downto 0);
35             EN                : out STD_LOGIC;
36             RS                : out STD_LOGIC;
37             D_BUS            : out STD_LOGIC_VECTOR (3 downto 0));
38
39
40 end LCD_CTRL;
41
42 architecture Behavioral of LCD_CTRL is
43
44     signal old_val      : std_logic_vector (7 downto 0) := "00000000";
45     signal counter      : integer range 0 to 70;
46
47 begin
48
49     -- RS high data / RS low command
50
51     process (CLOCK)
52     begin
53
54
55         if( rising_edge(CLOCK) and LCD_DATA /= old_val and ENABLE = '1') then
56
57             counter <= counter + 1;
58
59             case counter is
60
61                 when 11 =>
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```
62     RS      <= '1';
63     EN      <= '0';
64     D_BUS(0) <= LCD_DATA(4); --DB4
65     D_BUS(1) <= LCD_DATA(5); --DB5
66     D_BUS(2) <= LCD_DATA(6); --DB6
67     D_BUS(3) <= LCD_DATA(7); --DB7
68
69     when 12 =>
70     EN      <= '1';
71     D_BUS(0) <= LCD_DATA(4); --DB4
72     D_BUS(1) <= LCD_DATA(5); --DB5
73     D_BUS(2) <= LCD_DATA(6); --DB6
74     D_BUS(3) <= LCD_DATA(7); --DB7
75
76     when 13 =>
77     EN      <= '0';
78     D_BUS(0) <= LCD_DATA(0); --DB0
79     D_BUS(1) <= LCD_DATA(1); --DB1
80     D_BUS(2) <= LCD_DATA(2); --DB2
81     D_BUS(3) <= LCD_DATA(3); --DB3
82
83     when 14 =>
84     EN      <= '1';
85     D_BUS(0) <= LCD_DATA(0); --DB0
86     D_BUS(1) <= LCD_DATA(1); --DB1
87     D_BUS(2) <= LCD_DATA(2); --DB2
88     D_BUS(3) <= LCD_DATA(3); --DB3
89
90     when 15 =>
91     EN      <= '0';
92     D_BUS <= "0000";
93
94     when 65 =>
95     EN      <= '0';
96     D_BUS <= "0000";
97     counter <= 0;
98     old_val <= LCD_DATA;
99
100    when others =>
101    end case;
102
103    end if;
104    end process;
105    End Behavioral;
106
107
```