

Table 2-1. 8558B Mainframe Interconnections

Pin on P1	Signal or Voltage
1	CRT HORIZ Adjustment Signal
2	GROUND from Mainframe (jumpered to Pin 8 of P1)
3	N.C.
4	N.C.
5	AUX D Horizontal Output to mainframe rear-panel (labeled EXT. RESET on 183A/B/C/D).
6	N.C.
7	N.C.
8	GROUND from mainframe (jumpered to Pin 2 of P1)
9	N.C.
10	N.C.
11	AUX D Horizontal Output to mainframe rear panel
12	AUX C 21.4 MHz IF Output to mainframe rear panel
13	AUX B Pen Lift/Blanking Output to mainframe rear panel
14	AUX A Vertical Output to mainframe rear panel
15	GROUND
16	N.C.
17	BLANKING
18	N.C.
19	GROUND from mainframe (jumpered to Pin 24 of P1)
20	N.C.
21	BEAM FINDER circuit
22	N.C.
23	N.C.
24	GROUND from mainframe (jumpered to Pin 19 of P1)
25	N.C.
26	N.C.
27	N.C.
28	-12.6 Vdc from mainframe
29	+15 Vdc from mainframe
30	+100 Vdc from mainframe
31	20 VAC from mainframe (Line sync.)
32	N.C.
W10P3 (2 contacts)	Vertical deflection to CRT